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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,639	09/30/2003	Nobuya Matsubara	JP920020184US1	7854

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EXAMINER	
FIGUEROA, NATALIA	

ART UNIT	PAPER NUMBER
2651	

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,639	MATSUBARA ET AL.	
	Examiner	Art Unit	
	Natalia Figueroa	2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6-10 and 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Saiki et al (USPN 5,677,802), hereinafter Saiki.

Regarding claim 1, Saiki discloses a data storage device based on a magnetic recording Medium (abstract, fig. 17 and col. 1, lines 36-37), comprising a magnetic head for reading magnetic information recorded on said magnetic recording medium and acquiring a read signal (fig. 17 and col. 1, lines 36-38); a data read means for converting said read signal read by said magnetic head into desired data in synchronism with a read clock signal (fig. 17 and col. 1, lines 40-50); and a read clock control means for controlling the phase of said read clock signal in accordance with the phase of said read signal read by said magnetic head (or VCO circuit, fig. 17 and col. 1, line 61-col. 2, line 7).

Regarding claim 2, Saiki further discloses that said read clock control means comprises an oscillation means for generating said read clock signal and a correction means for controlling said oscillation means in such a manner as to recognize the phase difference between the read clock signal generated by said oscillation means and said read signal and adjust the phase of the read clock signal for the phase of the read signal (col. 3, lines 18-21 and 50-53 and col. 4, lines 9-30)

Regarding claim 3, Saiki further discloses that said data read means and said read clock control means are furnished as the functions of a read/write channel (or R/W amplifier and VCO circuit, fig. 17 and col. 1, line 39 and 64-65).

Regarding claim 4, Saiki further discloses a storage means for storing the information about the phase of said read signal (fig. 1 and col. 7, line 61-col. 8, line 15); wherein said read clock control means corrects the phase of said read clock signal in accordance with the information about the phase of said read signal, which is stored in said storage means, if the phase difference between said read signal and said read clock signal is greater than predefined (or phase adjustment, col. 8, lines 19-36).

Regarding claim 6, Saiki further discloses that said storage means is a memory provided for a hard disk controller (fig. 1 and col. 8, line 5).

Regarding claim 7, Saiki further discloses that if data is not successfully read due to a phase difference between said read clock signal and said read signal, said data read means sets a window at a position at which the data has not been successfully read, and wherein the read clock signal whose phase is controlled by said read clock control means is used within the window to read the data again (or playback signal, col. 1, lines 34-61).

Regarding claim 8, Saiki further discloses that if data is not successfully read due to a phase difference between said read clock signal and said read signal, said data read means uses the read clock signal whose phase is controlled by said read clock control means to perform a data read again at a position at which the data has not been successfully read (or playback signal, col. 11, lines 38-50 and col. 12, lines 5-15).

Regarding claim 9, Saiki discloses a correction mechanism for correcting the operation performed in a process for reading data written on a predefined recording medium, the correction mechanism comprising; a phase detector for detecting the phase of a read signal which is obtained by reading the information recorded on said recording medium (abstract and col. 8, line 23-26); an oscillator for generating a read control signal which converts said read signal into desired data (or clock signal, col. 8, lines 30-32); and a phase corrector for controlling said oscillator in accordance with the phase of said read signal, which is detected by said phase detector, in order to correct the phase of the read control signal generated by said oscillator (or phase adjustment, col. 8, lines 32-36).

Regarding claim 10, Saiki further discloses that said phase corrector compares the phase of said read signal, which is detected by said phase detector, against the phase of said read control signal, which is generated by said oscillator, and shifts the phase of the read control signal until it coincides with the phase of the read signal (or synchronously, col. 8, lines 23-36 and col. 10, lines 18-24).

Regarding claim 12, Saiki further discloses said phase detector, said oscillator, and said phase corrector form a control loop for exercising feedback control over the read control signal during a data read process (fig. 1 and col. 8, lines 23-36).

Regarding claim 13, method claim 13 is drawn to the method of using the corresponding apparatus claimed in claims 1-2. Therefore method claim 13 corresponds to apparatus claims 1-2 and is rejected for the same reasons of anticipation as used above.

Regarding claim 14, method claim 14 is drawn to the method of using the corresponding apparatus claimed in claims 7. Therefore method claim 14 corresponds to apparatus claim 7 and is rejected for the same reasons of anticipation as used above.

Regarding claim 15, method claim 15 is drawn to the method of using the corresponding apparatus claimed in claims 7-8. Therefore method claim 15 corresponds to apparatus claims 7-8 and is rejected for the same reasons of anticipation as used above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saiki in view of Muto et al (USPN 5,436,770), hereinafter Muto.

Regarding claim 5, Saiki is relied upon for the same reasons of rejection as stated above. Saiki fails to explicitly teach that storage means is a register provided for the read/write channel.

However, Muto disclose such in the (fig. 5 and col. 7, lines 13-16). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method as disclosed by Saiki with the above teachings from Muto to include a register or other storage means letting phase data be stored, therefore adjusting the phase as needed hence making it possible to read and write data.

Regarding claim 11, Saiki is relied upon for the same reasons of rejection as stated above. Saiki further discloses that if the phase difference between said read signal and said read control signal generated by said oscillator is greater than predefined, said phase corrector corrects the phase of the read control signal in accordance with the information about the phase of said read signal which is stored in said register (or phase adjustment, col. 8, lines 23-36). Saiki fails to explicitly teach a register for storing the information about the phase of said read signal which is detected by said phase detector.

However, Muto disclose such in the (fig. 5 and col. 7, lines 13-16). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method as disclosed by Saiki with the above teachings from Muto to include a register or other storage means letting phase data be stored, therefore adjusting the phase as needed hence making it possible to read and write data.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents are cited to further show the state of the art with respect to data read correction and control in a data storage device.

a) IBM Technical Disclosure Bulletin (NN80013803): Discloses a phase-locked system.

b) Spagna (IEEE: Phase Locked Loop...): Discloses phase locked loop delay compensation techniques.

c) Du et al (IEEE: A Linearly Constrained...): Discloses interaction between a FIR filter, and AGC and PLL.

d) Fujimoto (JP 10-027435): Discloses a phase error detecting circuit.

e) Vishakhadatta et al (USPN 6,028,727): Discloses read channel circuits.

f) Honma (USPN 6,788,484): Discloses a PLL circuit.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Natalia Figueroa whose telephone number is (703) 305-1260. The examiner can normally be reached on Monday - Thursday 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh N. Tran can be reached on (703) 305-4040. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER